

EE 435

Lecture 17

Compensation of Feedback Amplifiers
Two-Stage Op Amp Design Strategies

Compensation

Compensation is the manipulation of the poles and/or zeros of the open-loop amplifier so that when feedback is applied, the closed-loop circuit will perform acceptably

Acceptable performance is often application dependent and somewhat interpretation dependent

Acceptable performance should include effects of process and temperature variations

Although some think of compensation as a method of maintaining stability with feedback, acceptable performance generally dictates much more stringent performance than simply stability

Compensation criteria are often an indirect indicator of some type of desired (but unstated) performance

Varying approaches and criteria are used for compensation often resulting in similar but not identical performance

Over compensation often comes at a considerable expense (increased power, decreased frequency response, increased area, ...)

Nyquist Plots

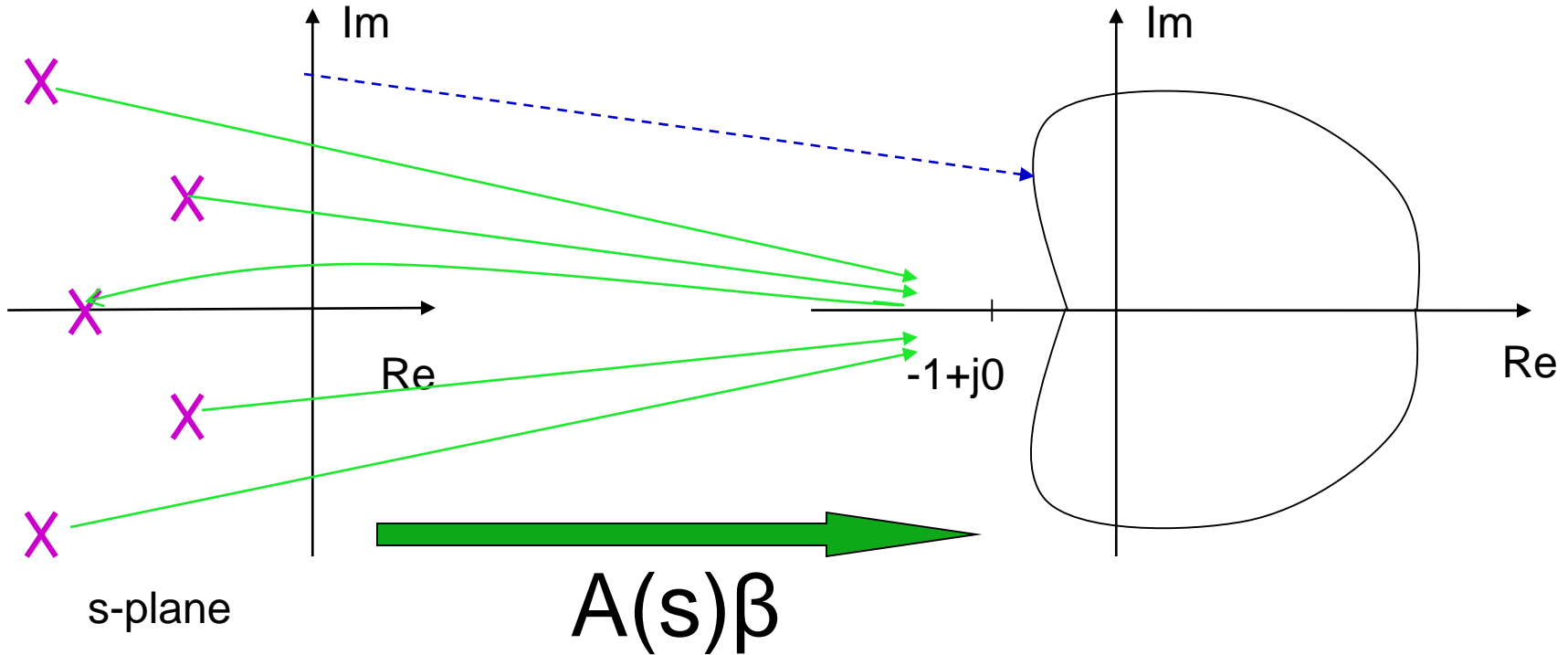
The Nyquist Plot is a plot of the Loop Gain ($A\beta$) versus $j\omega$ in the complex plane for $-\infty < \omega < \infty$

Theorem: A system is stable iff the Nyquist Plot does not encircle the point $-1+j0$.

Note: If there are multiple crossings of the real axis by the Nyquist Plot, the term encirclement requires a formal definition that will not be presented here

Nyquist Plots

$$D_{FB}(s) = 1 + A(s)\beta(s)$$



$-1+j0$ is the image of ALL poles

The Nyquist Plot is the image of the entire imaginary axis and separates the image complex plane into two parts

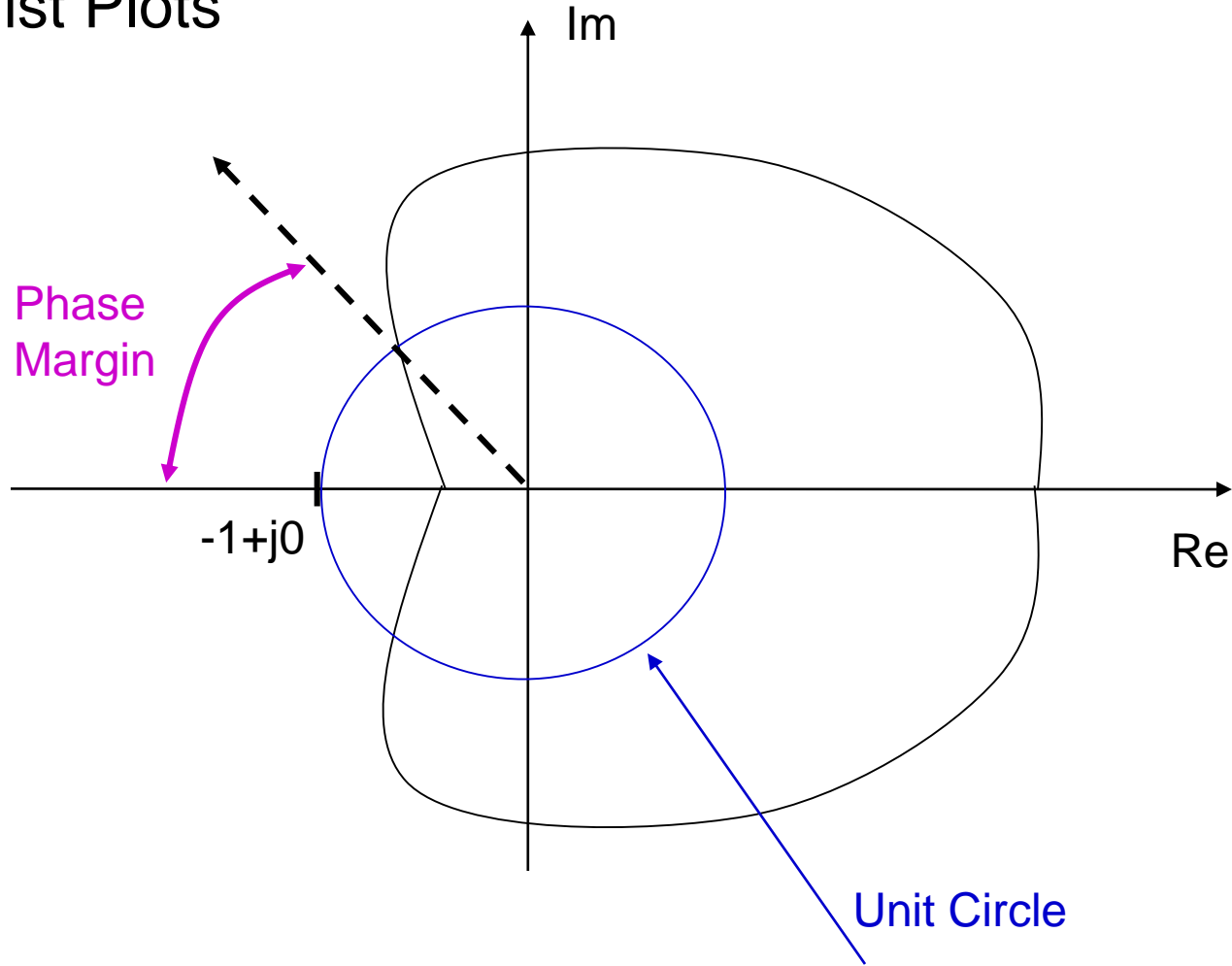
Everything outside of the Nyquist Plot is the image of the LHP

Nyquist plot can be generated with pencil and paper



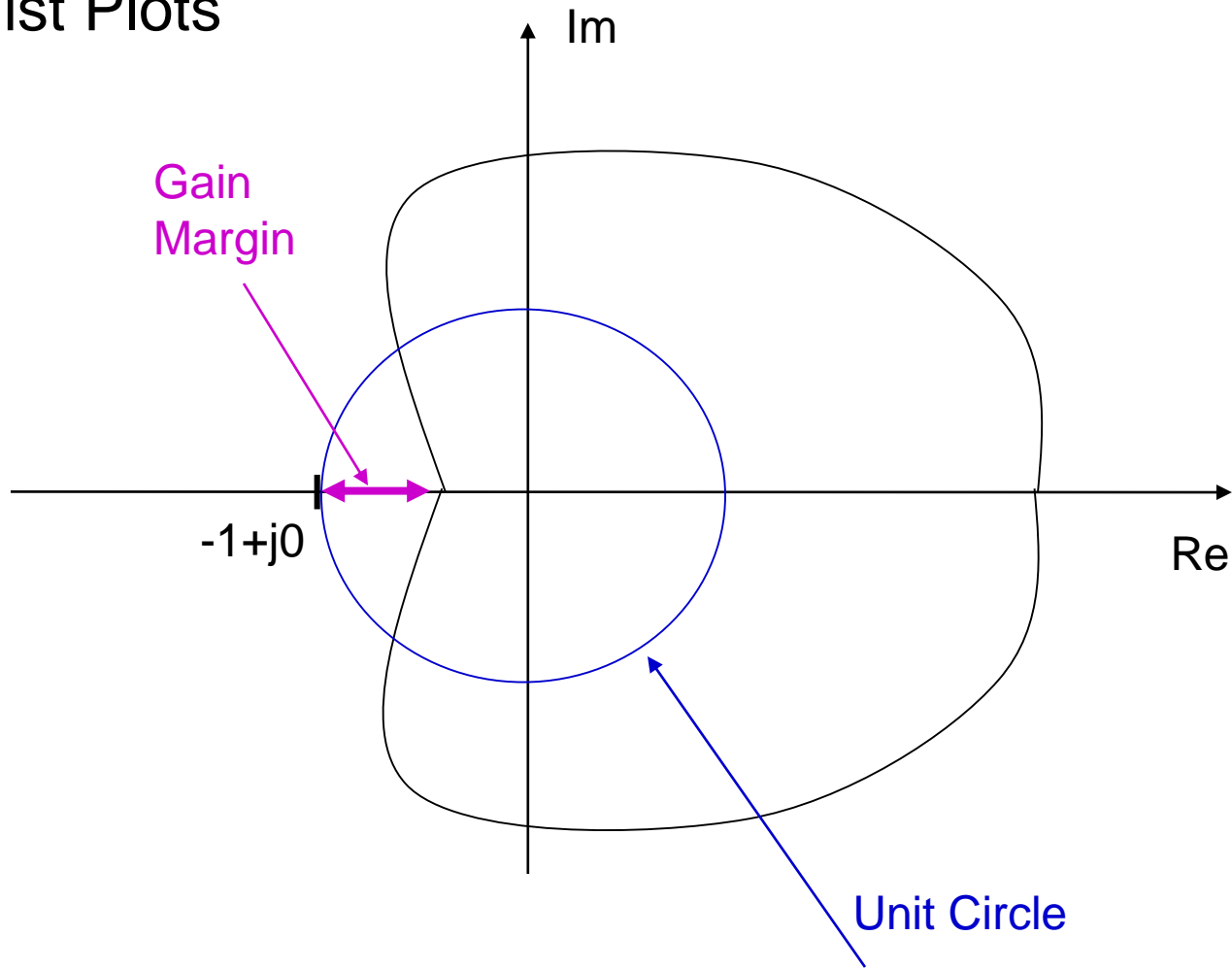
Important in the '30s - '60's

Nyquist Plots



Phase margin is $180^\circ - \text{angle of } A\beta \text{ when the magnitude of } A\beta = 1$

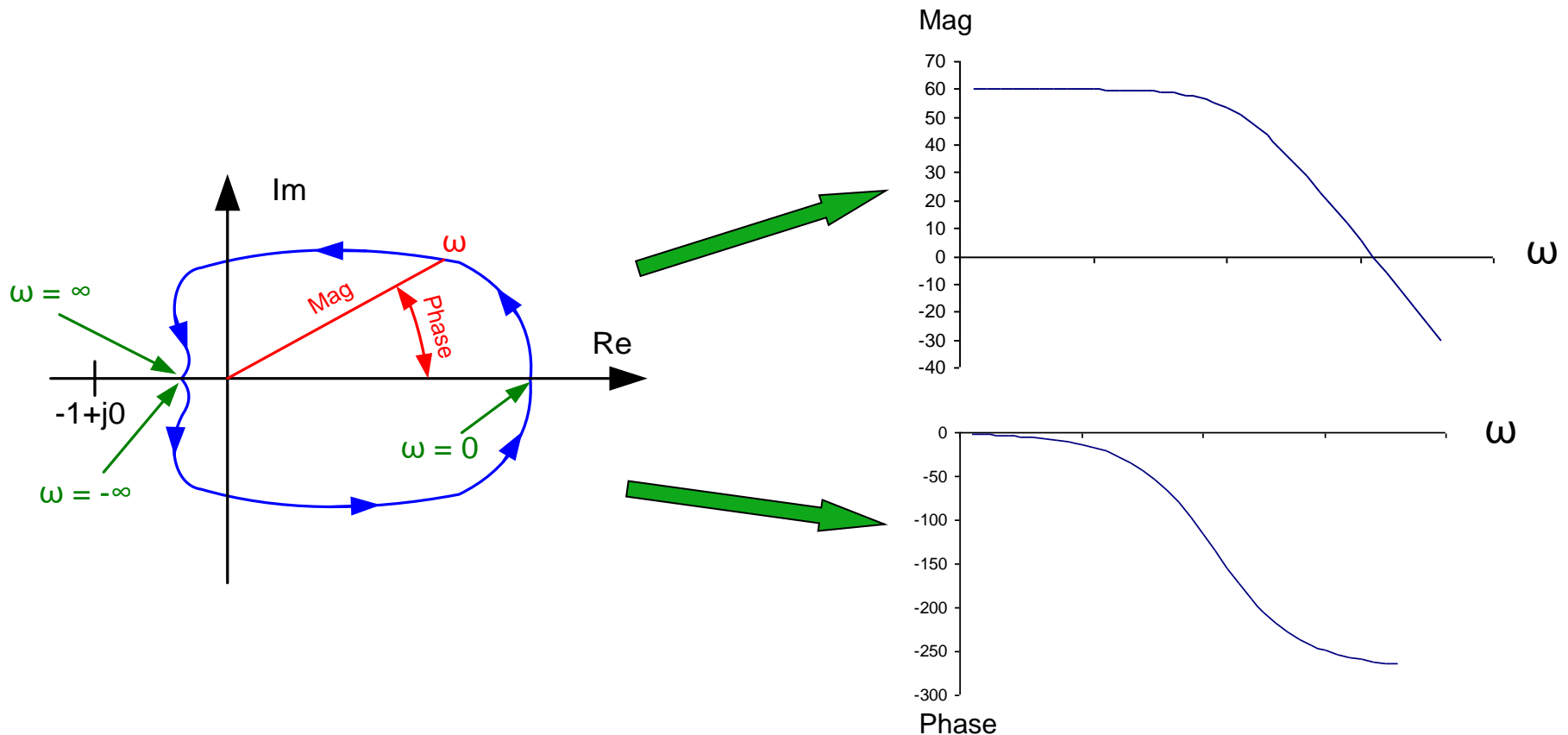
Nyquist Plots



Gain margin is $1 - \text{magnitude of } A\beta \text{ when the angle of } A\beta = 180^\circ$

Nyquist and Gain-Phase Plots

Nyquist and Gain-Phase Plots convey identical information but gain-phase plots often easier to work with

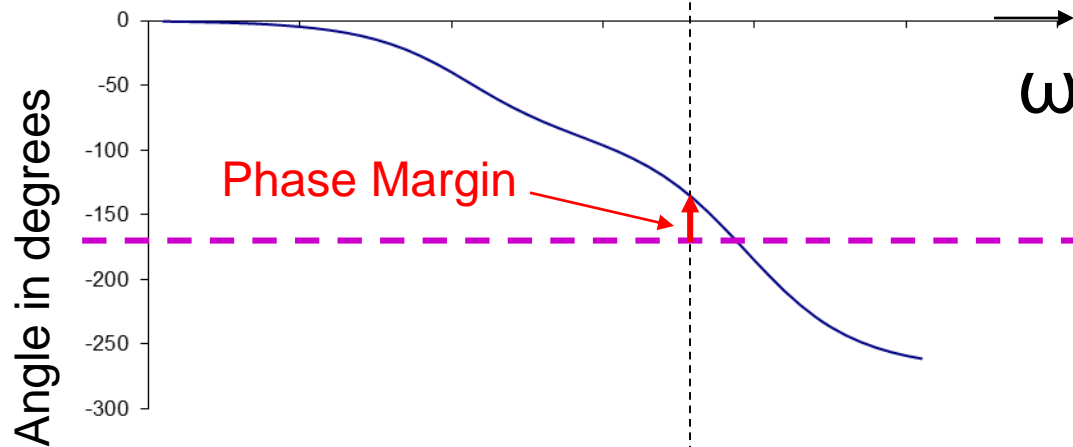
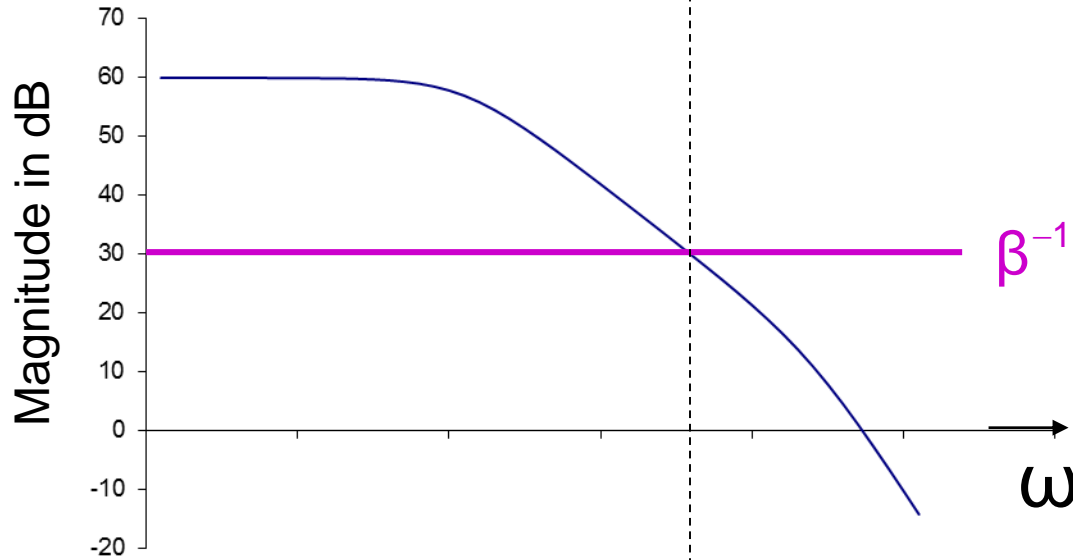


Note: The two plots do not correspond to the same system in this slide

Gain and Phase Margin Examples

$$A(s) = \frac{1000}{(s+1)\left(\frac{s}{200} + 1\right)}$$

$$\beta = .031$$



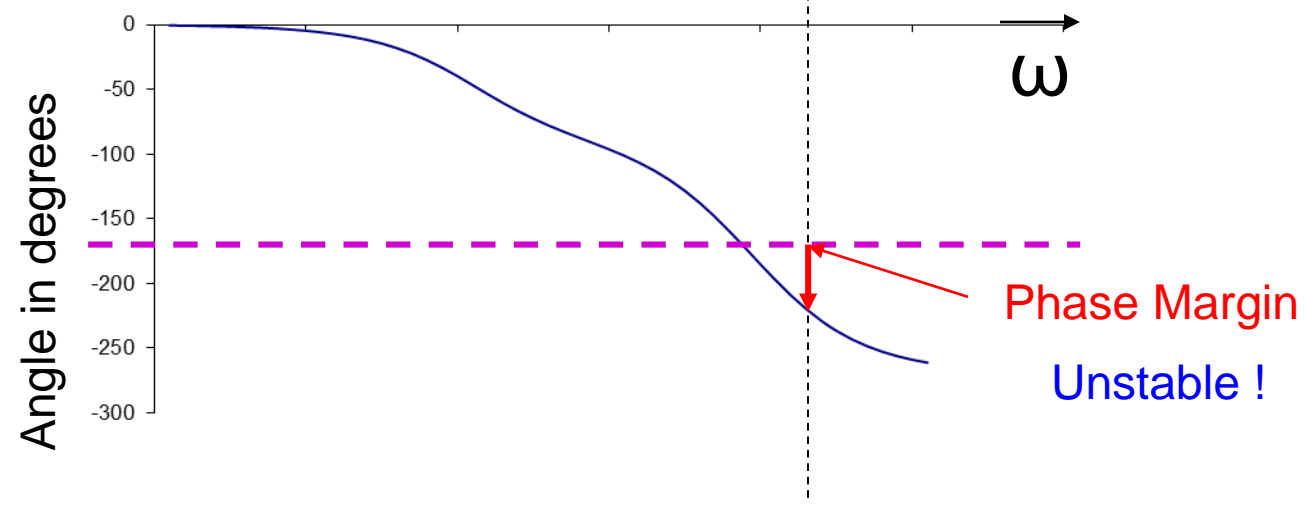
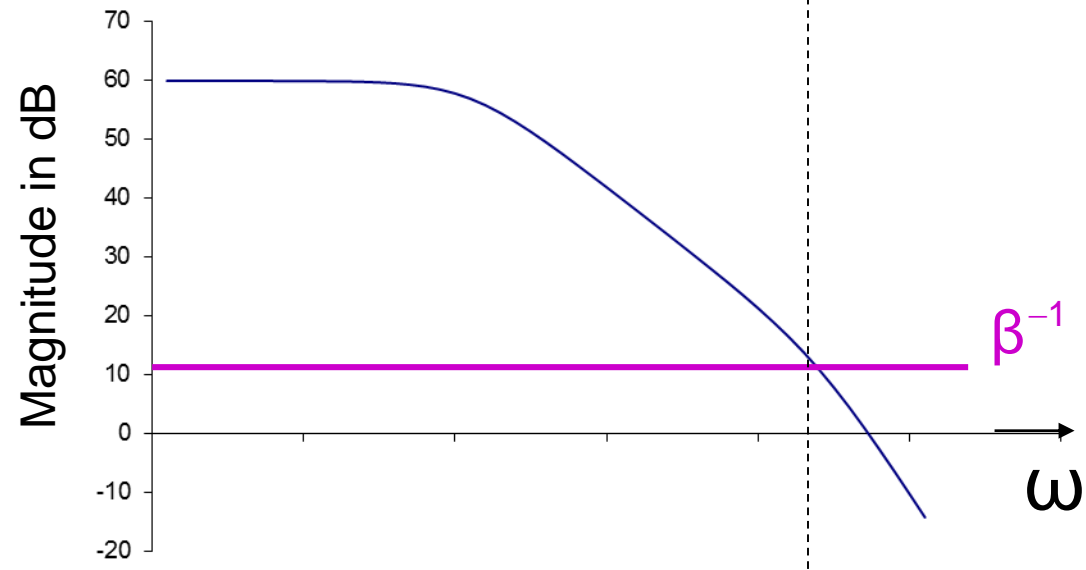
Stable !

But is it a good compensation ?

Gain and Phase Margin Examples

$$A(s) = \frac{1000}{(s+1)\left(\frac{s}{200} + 1\right)}$$

$$\beta = .31$$



Relationship between pole Q and phase margin

In general, the relationship between the phase margin and the pole Q is dependent upon the order of the transfer function and on the location of the zeros

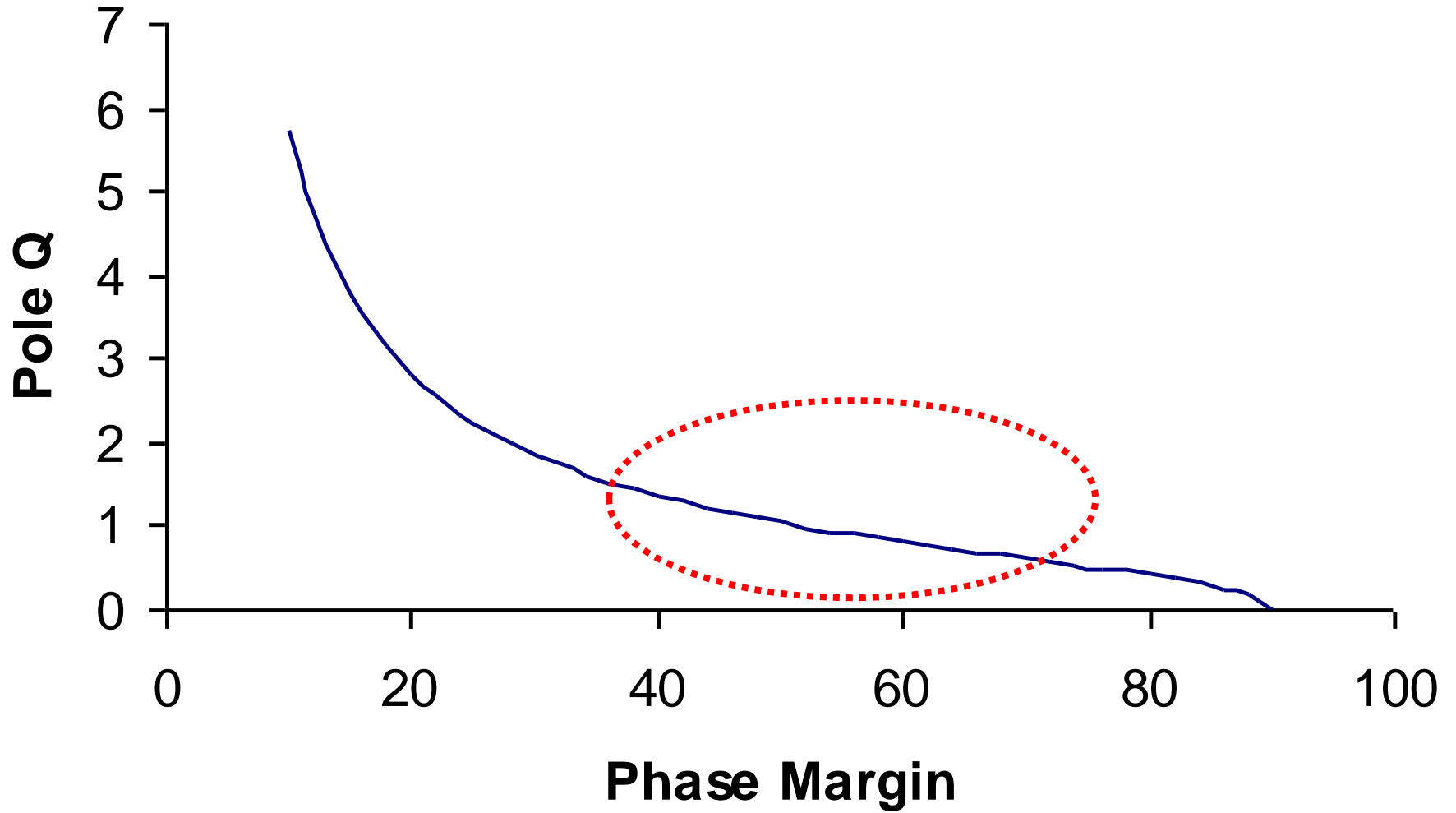
In the special case that the open loop amplifier is second-order low-pass, a closed form analytical relationship between pole Q and phase margin exists and this is independent of A_0 and β .

$$Q = \frac{\sqrt{\cos(\varphi_M)}}{\sin(\varphi_M)} \quad \varphi_M = \cos^{-1} \left(\sqrt{1 + \frac{1}{4Q^4}} - \frac{1}{2Q^2} \right)$$

The region of interest is invariable only for $0.5 < Q < 0.7$
larger Q introduces unacceptable ringing and settling
smaller Q slows the amplifier down too much

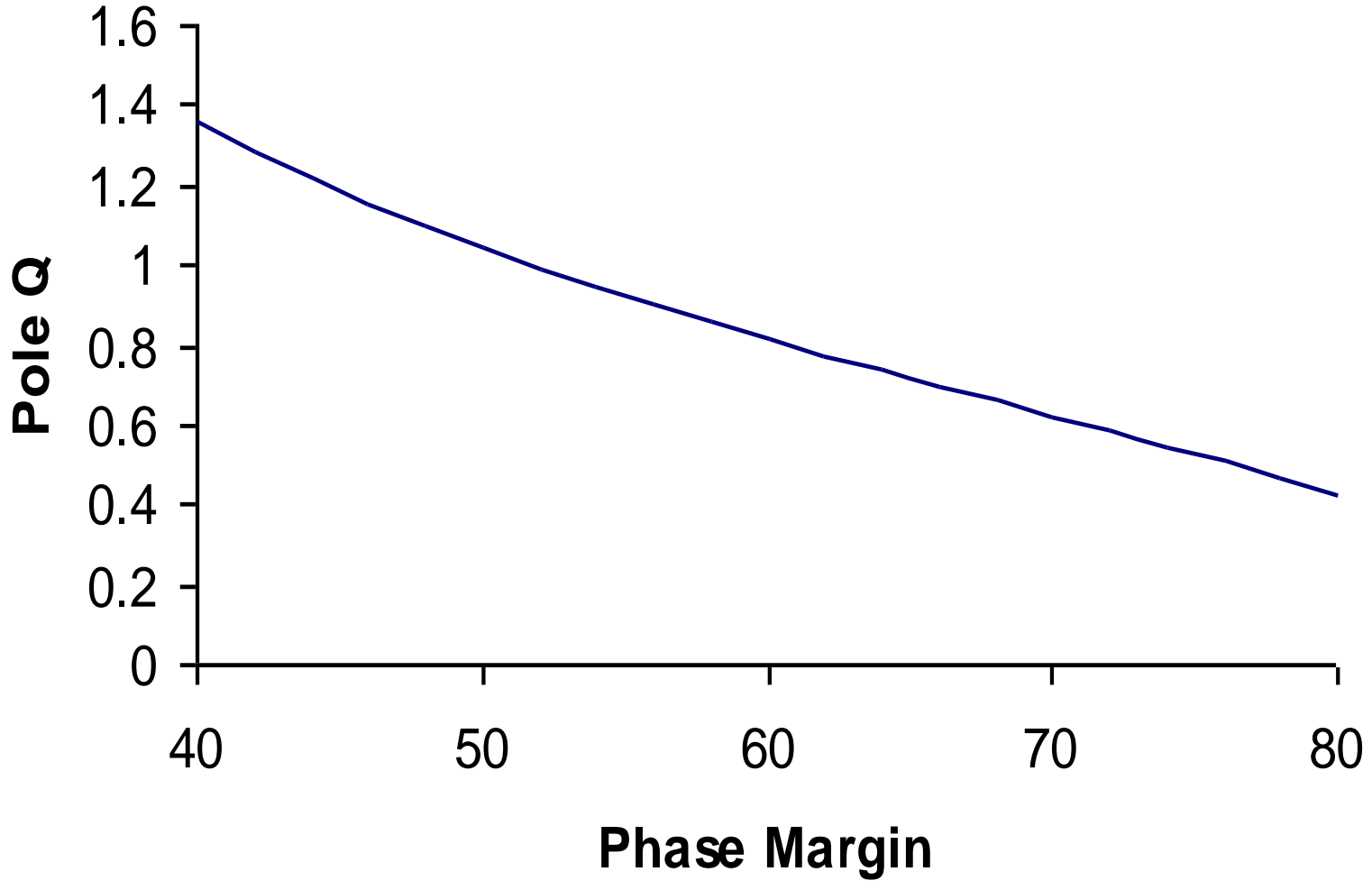
Phase Margin vs Q

Second-order low-pass Amplifier



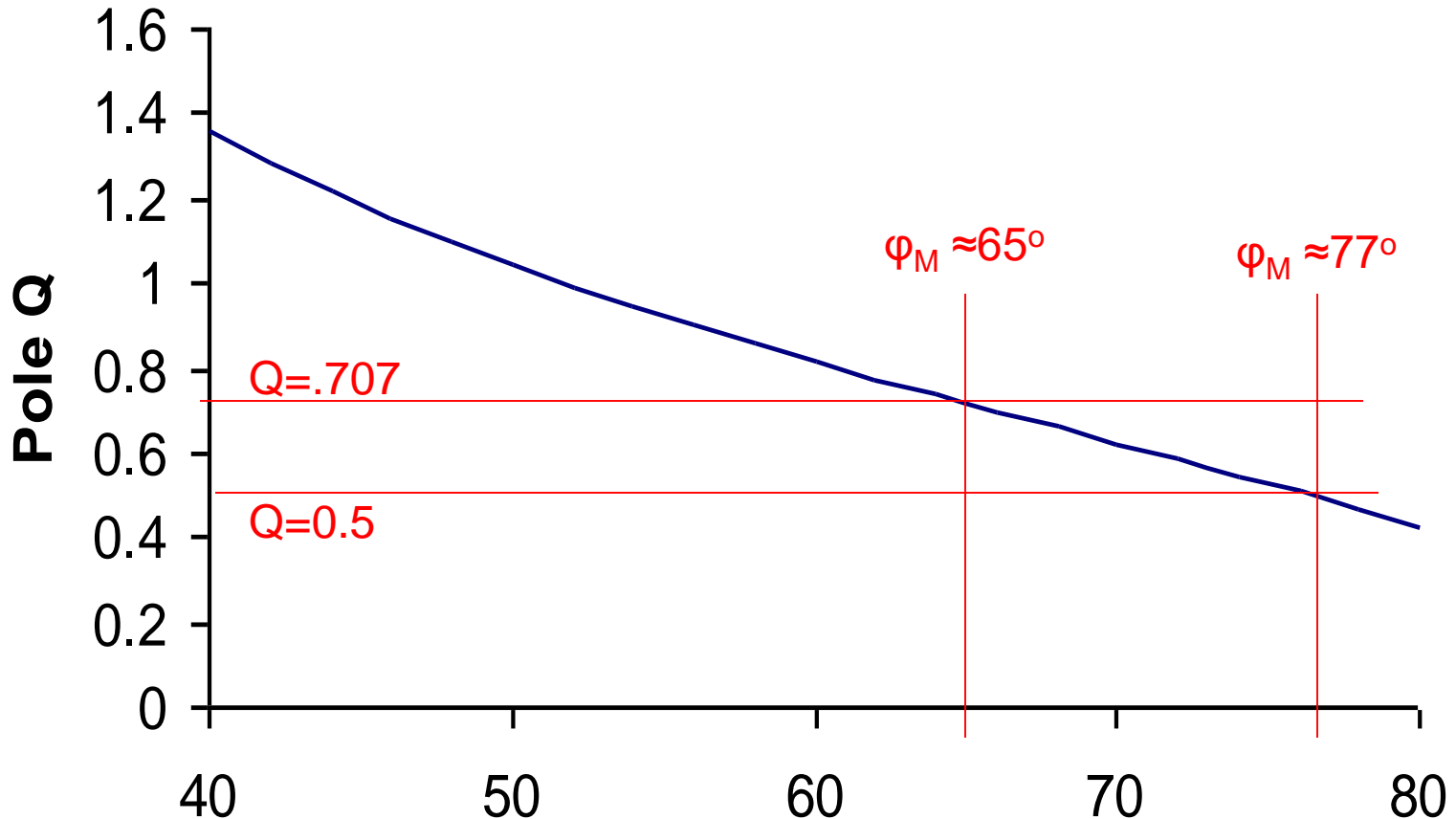
Phase Margin vs Q

Second-order low-pass Amplifier



Phase Margin vs Q

Second-order low-pass Amplifier



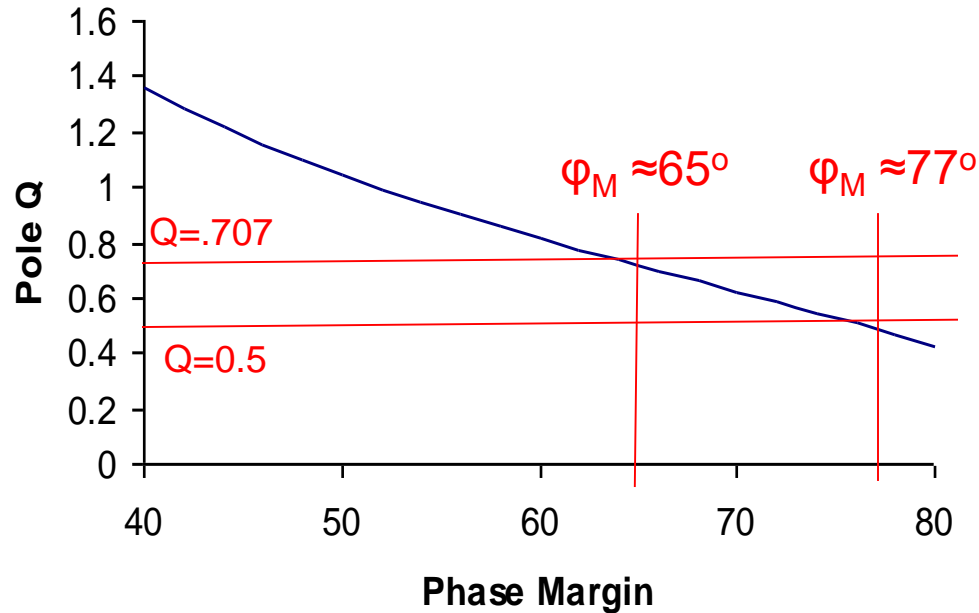
$.707 < Q < 0.5$



$65^\circ < \varphi_M < 75^\circ$

Phase-Margin Compensation Criteria

Phase Margin vs Q



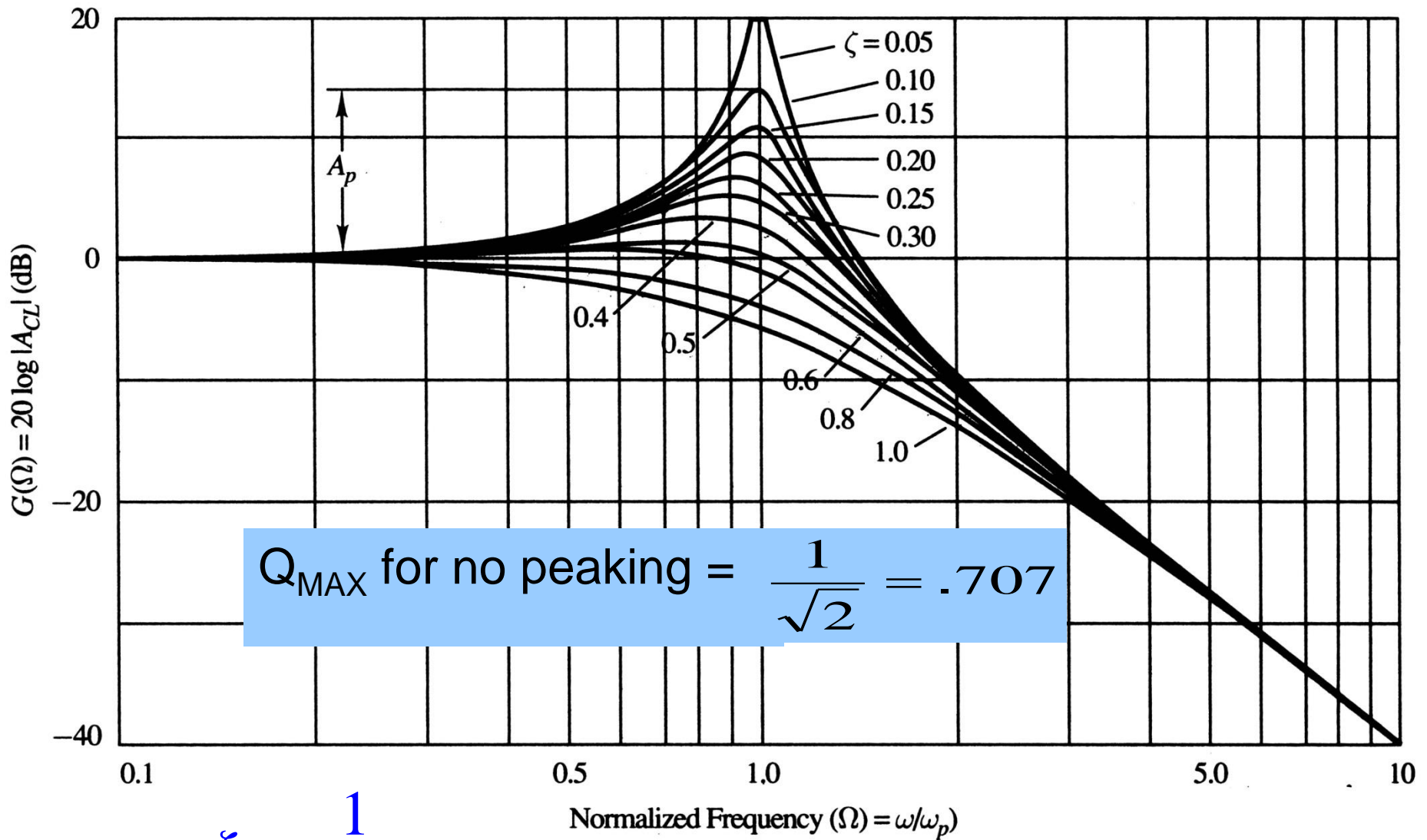
$.707 < Q < 0.5$



$65^\circ < \phi_M < 75^\circ$

- This relationship holds only for 2nd-order low-pass open loop amplifiers
- Considerable evidence of use of these phase margin criteria when not 2nd-order low-pass but not clear what relevance this may have for FB performance

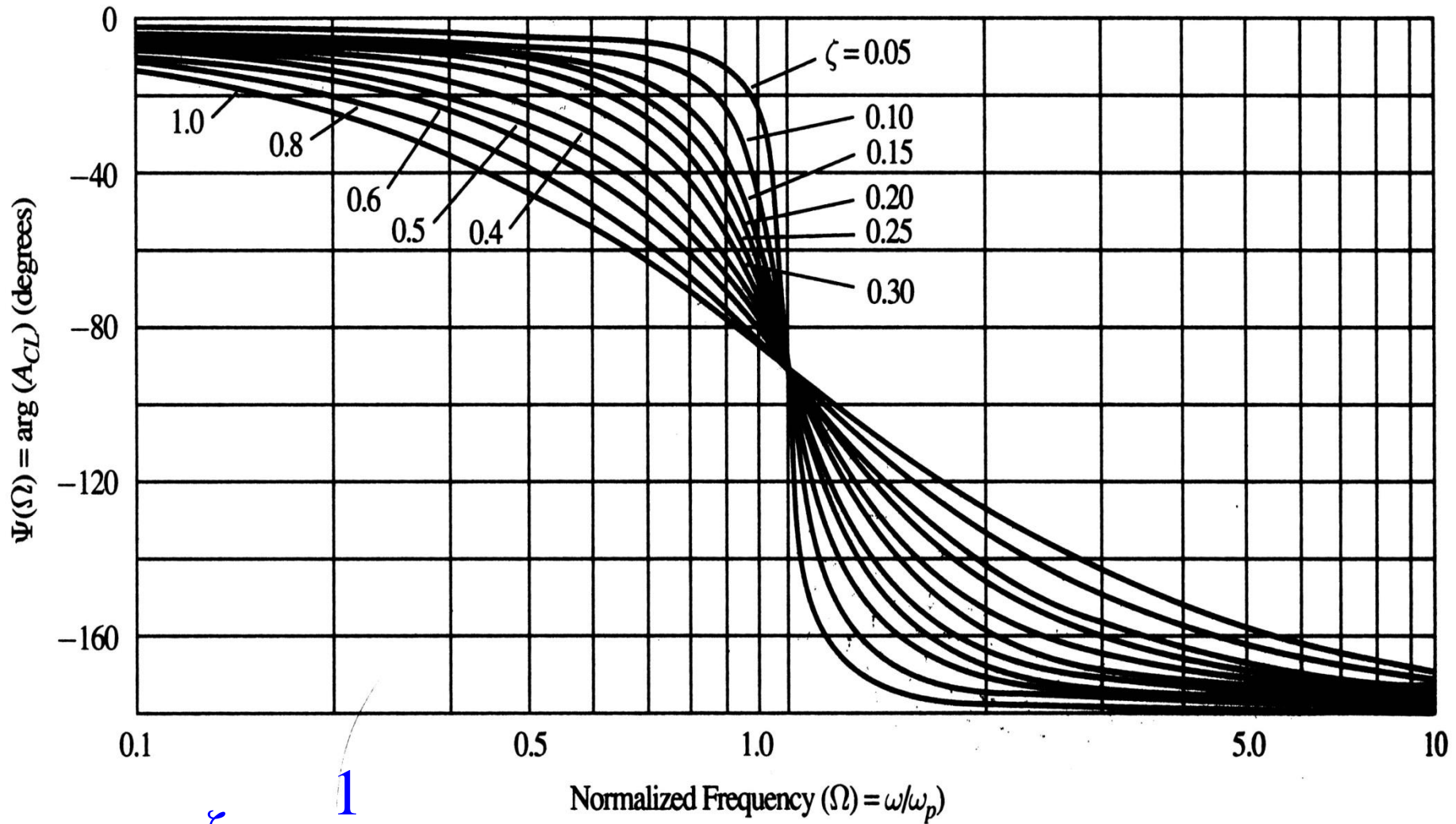
Magnitude Response of 2nd-order Lowpass Function



$$\zeta = \frac{1}{2Q}$$

From Laker-Sansen Text

Phase Response of 2nd-order Lowpass Function

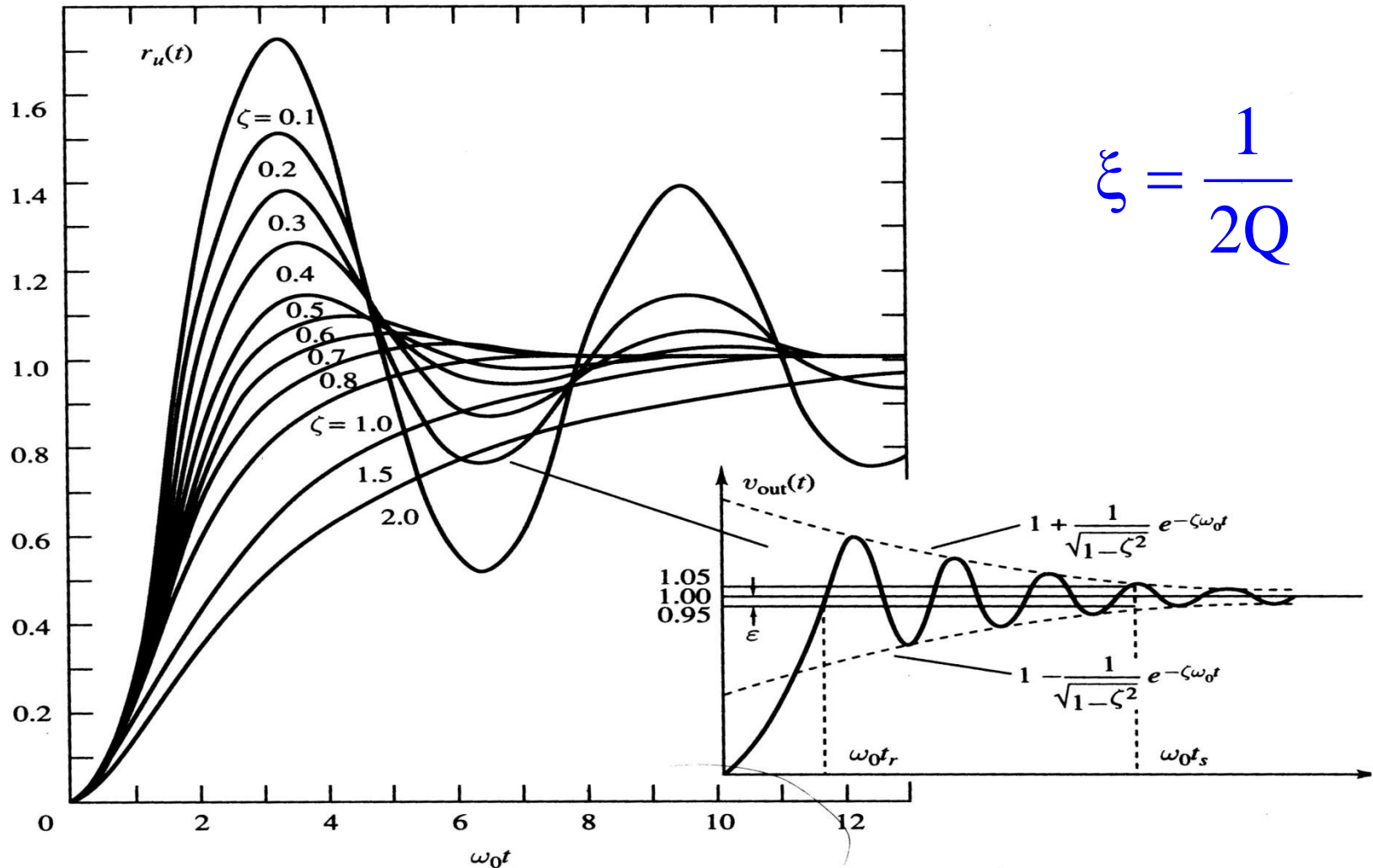


$$\zeta = \frac{1}{2Q}$$

(b)

From Laker-Sansen Text

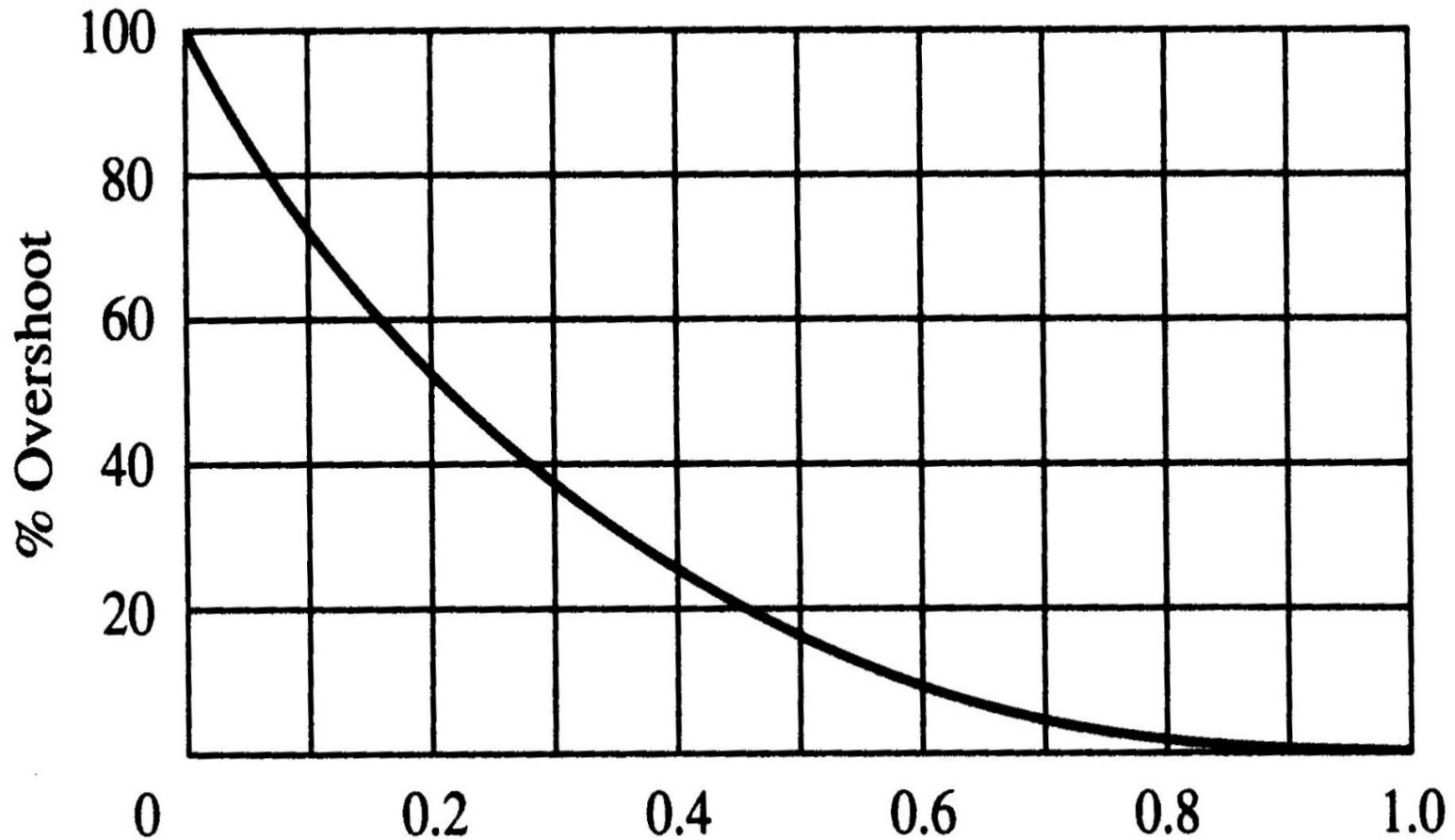
Step Response of 2nd-order Lowpass Function



$$\zeta = \frac{1}{2Q}$$

Q_{MAX} for no overshoot = 1/2

Step Response of 2nd-order Lowpass Function



$$\zeta = \frac{1}{2Q}$$

From Laker-Sansen Text

Compensation Summary

- Gain and phase margin performance often strongly dependent upon architecture
- Relationship between overshoot and ringing and phase margin were developed only for 2nd-order lowpass gain characteristics and differ dramatically for higher-order structures
- Absolute gain and phase margin criteria are not robust to changes in architecture or order
- It is often difficult to correctly “break the loop” to determine the loop gain $A\beta$ with the correct loading on the loop (will discuss this more later)

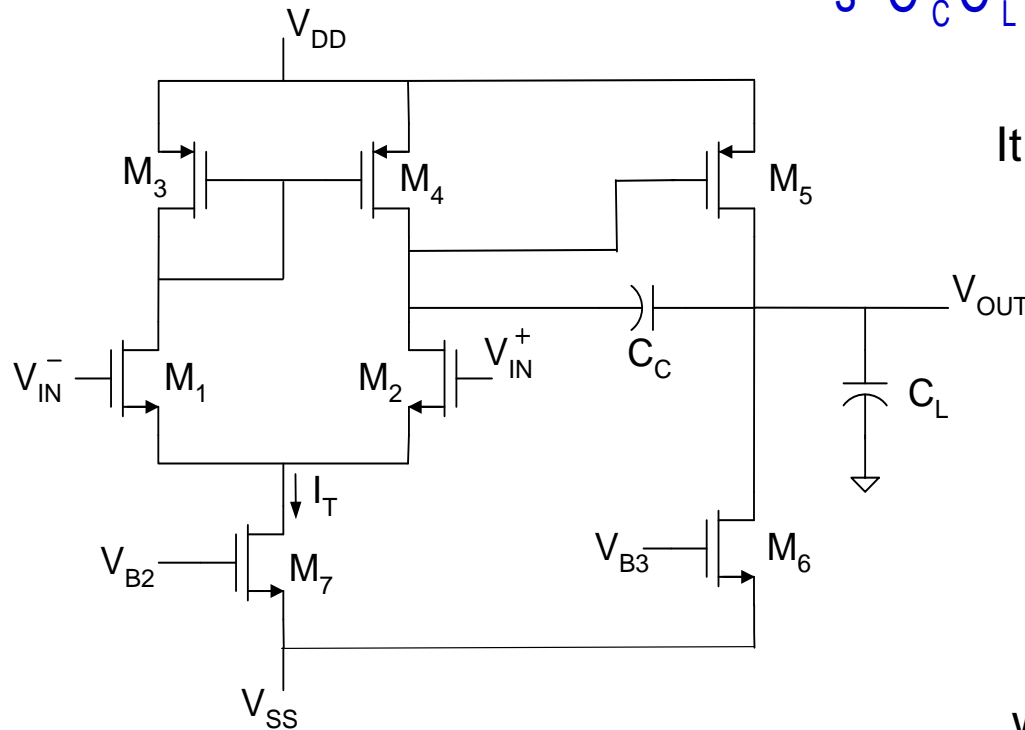
Design of Two-Stage Op Amps

- Compensation is critical in two-stage op amps
- General approach to designing two-stage op amps is common even though significant differences in performance for different architectures
- Will consider initially the most basic two-stage op amp with internal Miller compensation

Basic Two-Stage Op Amp

(with Miller compensation)

$$A_{FB}(s) \cong \frac{g_{md}(g_{mo} - sC_c)}{s^2 C_c C_L + s C_c (g_{mo} - \beta g_{md}) + \beta g_{md} g_{mo}}$$



It can be shown that

$$Q = \sqrt{\frac{C_L}{C_C}} \sqrt{\beta} \frac{\sqrt{g_{mo} g_{md}}}{g_{mo} - \beta g_{md}}$$

$$C_C = \frac{C_L \beta}{Q^2} \frac{g_{mo} g_{md}}{(g_{mo} - \beta g_{md})^2}$$

where $g_{md} = g_{m1}$ $g_{mo} = g_{m5}$

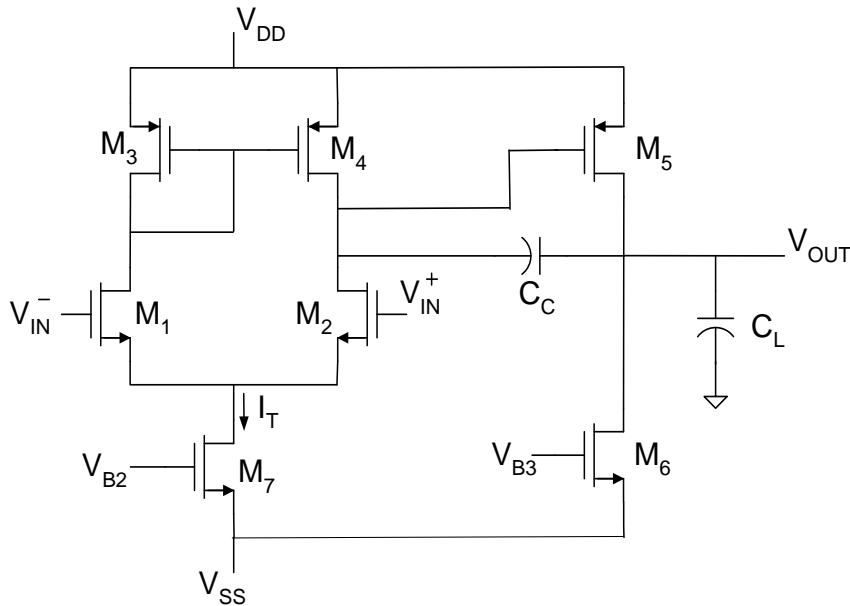
$g_{oo} = g_{o5} + g_{o6}$ and $g_{od} = g_{o2} + g_{o4}$

What pole Q is desired?

$.707 < Q < 0.5$

What phase margin is desired?

Basic Two-Stage Op Amp



Additional Performance Parameters
(from earlier analysis)

$$A(s) \cong \frac{g_{md}(g_{m0} - sC_C)}{s^2 C_C C_L + sC_C g_{m0} + g_{oo} g_{od}}$$

$$A_0 \cong \frac{g_{md} g_{m0}}{g_{oo} g_{od}}$$

$$BW \cong |p_1| \cong \frac{g_{oo} g_{od}}{g_{m0} C_C}$$

$$GB \cong \frac{g_{md}}{C_C}$$

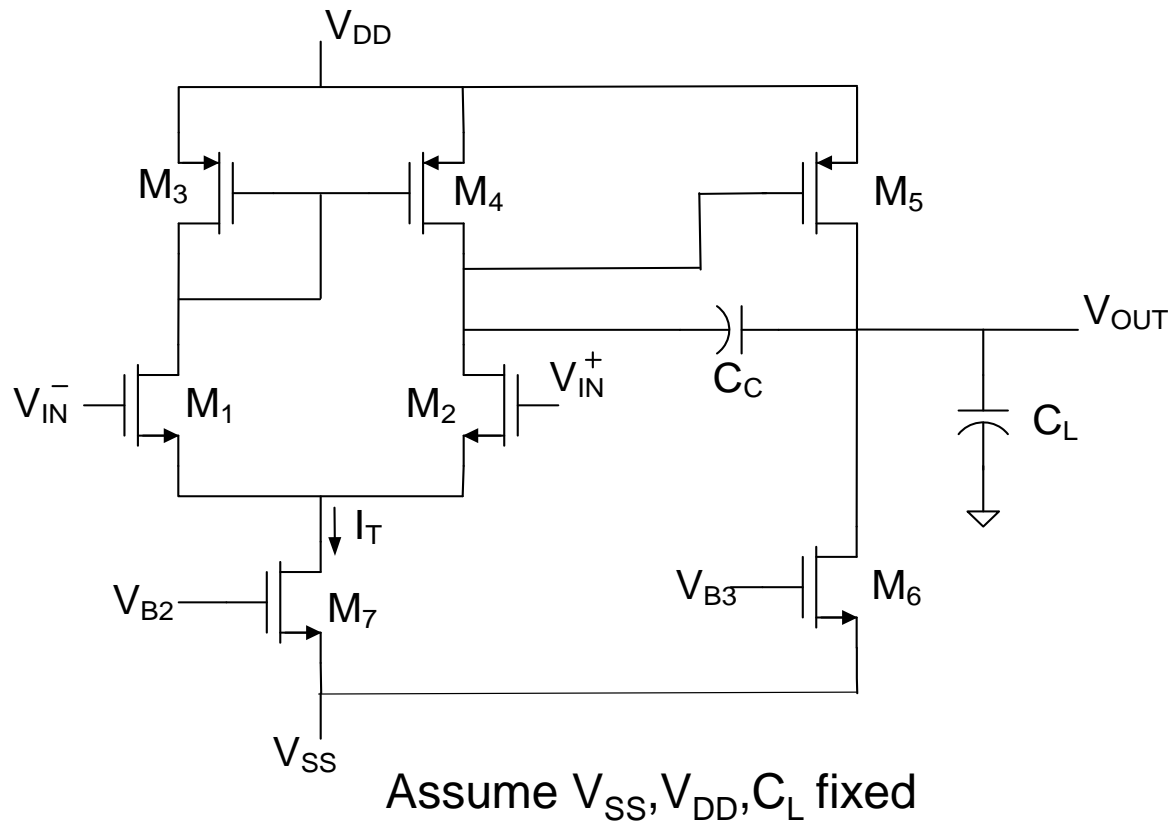
What is the SR?

Voltage at output of first stage changes little compared to V_{OUT}

$$SR = \left. \frac{dV_{OUT}}{dt} \right|_{\substack{I_{D4}=I_T \\ I_{D2}=0}} \cong \frac{dV_{C_C}}{dt} = \frac{I_T}{C_C}$$

$$SR \cong \frac{I_T}{C_C}$$

Natural Parameter Space for the Two-Stage Amplifier Design



$$S_{\text{NATURAL}} = \{W_1, L_1, W_3, L_3, W_5, L_5, W_6, L_6, W_7, L_7, I_T, I_{D6}, C_c\}$$

Design Degrees of Freedom

Total independent variables: 13

Degrees of Freedom: 13

If phase margin is considered a constraint

13 independent variables

1 constraint

12 degrees of freedom

Observation:

W,L appear as W/L ratio in almost all characterizing equations

Implication:

Degrees of Freedom are Reduced

$$S_{\text{NATURAL-REDUCED}} = \{(W/L)_1, (W/L)_3, (W/L)_5, (W/L)_6, (W/L)_7, I_{D6}, I_T, C_C\}$$

With phase margin constraint,

Degrees of freedom: 7

Common Performance Parameters of Operational Amplifiers (may be more of interest)

Parameter	Description
A_o	Open-loop DC Gain
GB	Gain-Bandwidth Product
Φ_m (or Q)	Phase Margin (or pole Q)
SR	Slew Rate
T_{SETTLE}	Settling Time
A_T	Total Area
A_A	Total Active Area
P	Power Dissipation
σ_{VOS}	Standard Deviation of Input Referred Offset Voltage (often termed the input offset voltage)
CMRR	Common Mode Rejection Ratio
PSRR	Power Supply Rejection Ratio
V_{imax}	Maximum Common Mode Input Voltage
V_{imin}	Minimum Common Mode Output Voltage
V_{omax}	Maximum Output Voltage Swing
V_{omin}	Minimum Output Voltage Swing
V_{noise}	Input Referred RMS Noise Voltage
S_v	Input Referred Noise Spectral Density

Common Performance Parameters

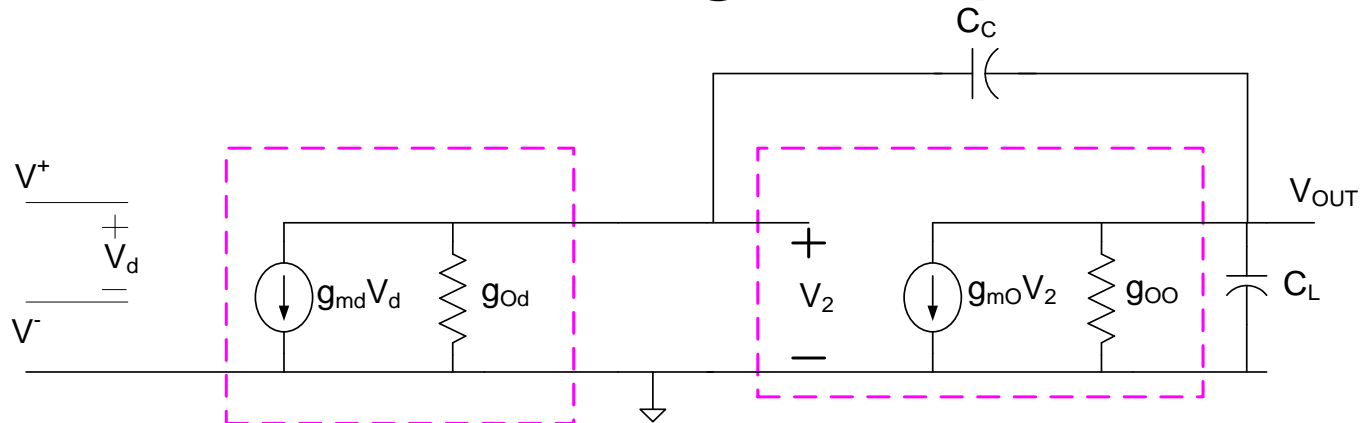
Total: 17

Performance parameters: 17

Degrees of freedom: 7

System is Generally Highly Over Constrained !

Typical Parameter Space for a Two-Stage Amplifier

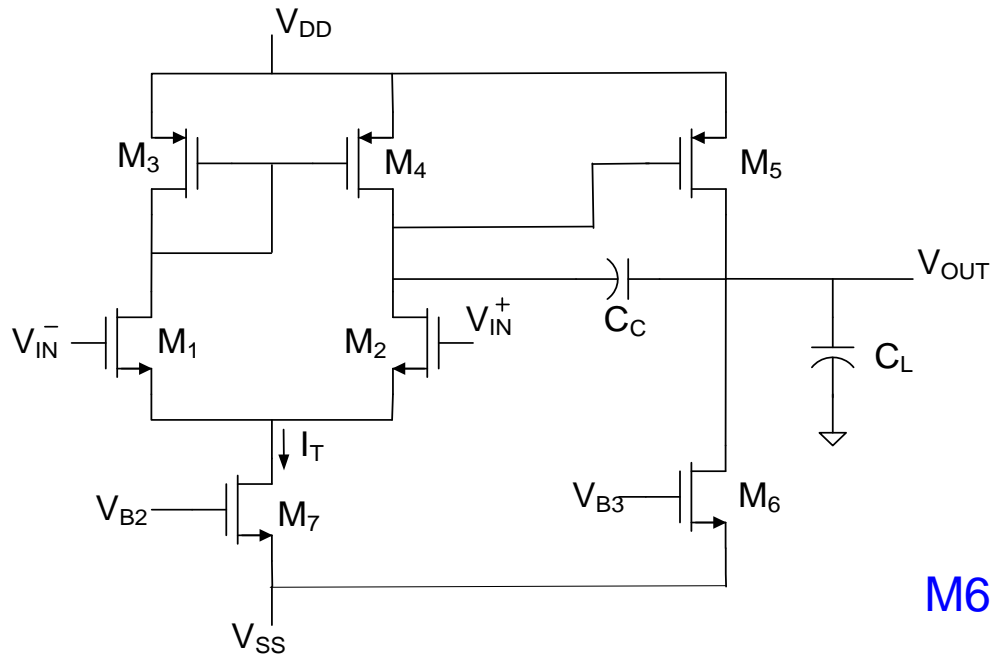


Small signal model of the two-stage operational amplifier

Small signal design parameters:

$$S_{\text{SMALL SIGNAL}} = \{g_{oo}, g_{od}, g_{mo}, g_{md}, C_C, g_{o2}, g_{o4}, g_{o5}, g_{o6}\}$$

Signal Swing of Two-Stage Op Amp



$$\text{M6:} \quad V_{\text{OUT}} > V_{\text{SS}} + V_{\text{EB6}}$$

$$\text{M5:} \quad V_{\text{OUT}} < V_{\text{DD}} - |V_{\text{EB5}}|$$

$$\text{M1:} \quad V_{\text{ic}} < V_{\text{DD}} + V_{\text{T1}} - |V_{\text{T3}}| - |V_{\text{EB3}}|$$

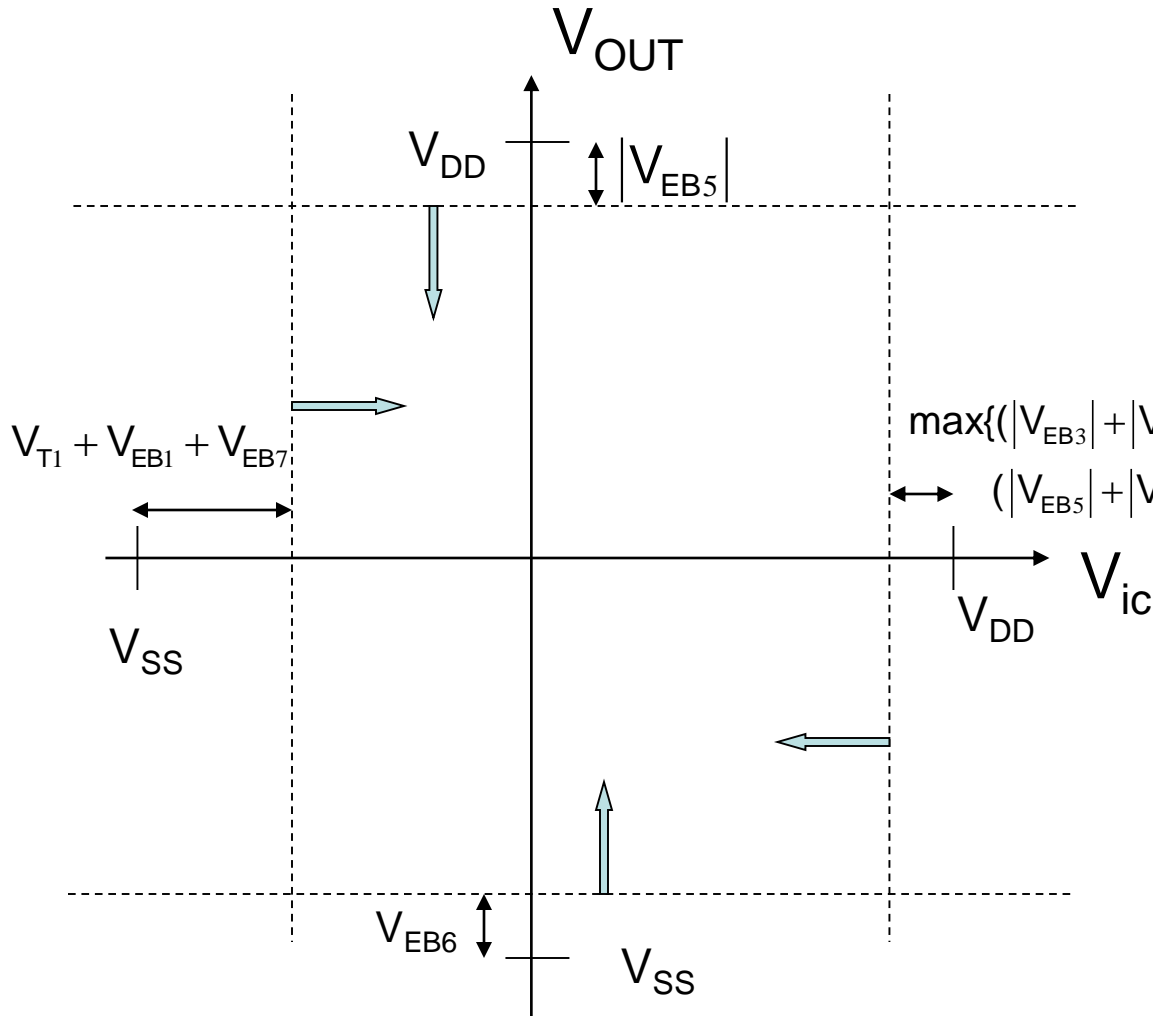
$$\text{M2:} \quad V_{\text{ic}} < V_{\text{DD}} + V_{\text{T1}} - |V_{\text{T5}}| - |V_{\text{EB5}}|$$

$$\text{M7:} \quad V_{\text{ic}} > V_{\text{T1}} + V_{\text{EB1}} + V_{\text{EB7}} + V_{\text{SS}}$$

$$S_{\text{swing/Bias Related}} = \{ C_{\text{C}}, V_{\text{EB1Q}}, V_{\text{EB3Q}}, V_{\text{EB5Q}}, V_{\text{EB6Q}}, V_{\text{EB7Q}}, I_{\text{T}} \}$$

Signal Swing of Two-Stage Op Amp

Graphical Representation



$$V_{OUT} < V_{DD} - |V_{EB5}|$$

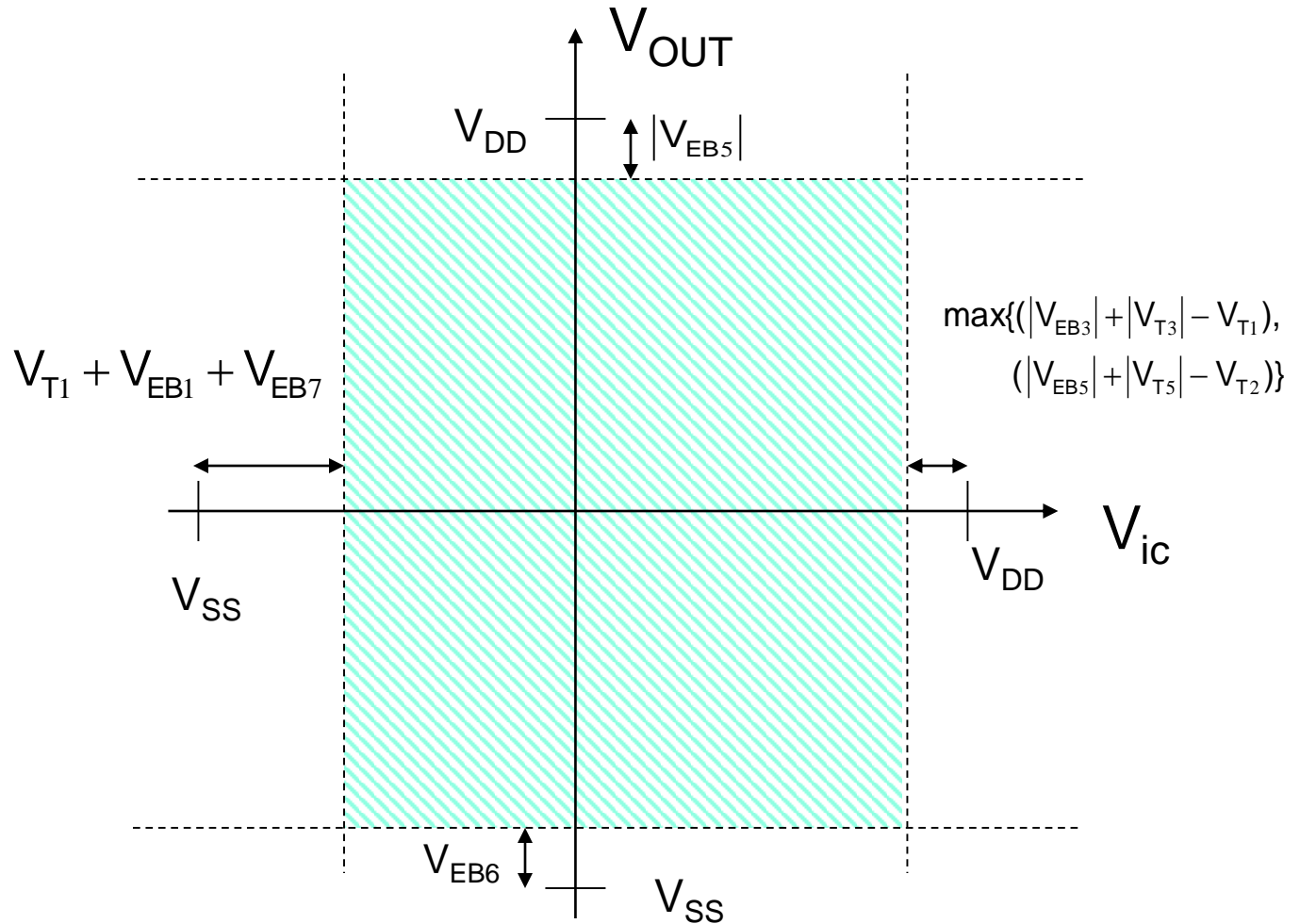
$$V_{OUT} > V_{SS} + V_{EB6}$$

$$V_{IC} > V_{T1} + V_{EB1} + V_{EB7} + V_{SS}$$

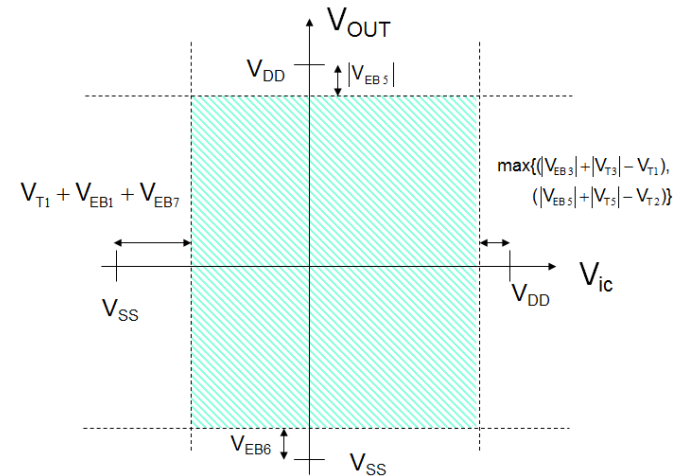
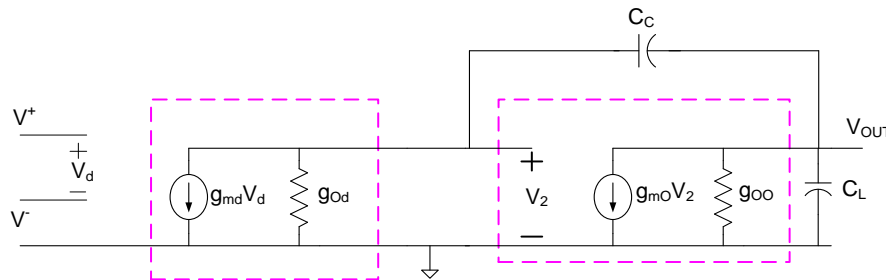
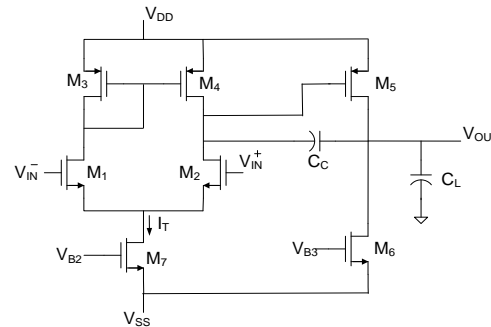
$$V_{IC} < V_{DD} + V_{T1} - |V_{T3}| - |V_{EB3}|$$

$$V_{IC} < V_{DD} + V_{T1} - |V_{T5}| - |V_{EB5}|$$

Signal Swing of Two-Stage Op Amp



Typical Parameter Space for a Two-Stage Amplifier



Augmented set of design parameters:

$$S_{\text{AUGMENTED}} = \{g_{oo}, g_{od}, g_{mo}, g_{md}, C_C, V_{EB1Q}, V_{EB3Q}, V_{EB5Q}, V_{EB6Q}, V_{EB7Q}, I_T, g_{o2}, g_{o4}, g_{o5}, g_{o6}\}$$

Parameters in this set are highly inter-related

Performance Parameter Summary for 7T Miller Compensated Op Amp

$$A_o \cong \frac{g_{md}g_{mo}}{g_{oo}g_{od}} \quad SR \cong \frac{I_T}{C_C} \quad GB \cong \frac{g_{md}}{C_C}$$

$$V_{OMAX} = V_{DD} - |V_{EB5}| \quad V_{OMIN} = V_{SS} + V_{EB6}$$

$$V_{inMIN} = V_{T1} + V_{EB1} + V_{EB7} + V_{SS}$$

$$V_{inMAX} = V_{DD} - \max\{(|V_{EB3}| + |V_{T3}| - V_{T1}), (|V_{EB5}| + |V_{T5}| - V_{T2})\}$$

Constraint:

$$C_C = \frac{C_L \beta}{Q^2} \frac{g_{mo}g_{md}}{(g_{mo} - \beta g_{md})^2}$$

$$S_{AUGMENTED} = \{g_{oo}, g_{od}, g_{mo}, g_{md}, C_C, V_{EB1Q}, V_{EB3Q}, V_{EB5Q}, \\ V_{EB6Q}, V_{EB7Q}, I_T, g_{o2}, g_{o4}, g_{o5}, g_{o6}\}$$

Parameter Inter-dependence

I_T affects

$$A_o \cong \frac{g_{md}g_{mo}}{g_{oo}g_{od}}$$
$$GB \cong \frac{g_{md}}{C_C}$$
$$SR \cong \frac{I_T}{C_C}$$
$$g_{md} \cong \frac{1}{2} \sqrt{\mu C_{OX} \frac{W_1}{L_1}} \sqrt{I_T}$$

The diagram illustrates the inter-dependence of circuit parameters. A central text 'I_T affects' has four blue arrows pointing to the equations above. The arrows point to the g_{md} term in the first equation, the g_{md} term in the second equation, the I_T term in the third equation, and the $\sqrt{I_T}$ term in the fourth equation.

A Set of Independent Design Parameters is Needed

Consider the Natural Reduced Parameter Set

$$\left\{ \frac{W_1}{L_1}, \frac{W_3}{L_3}, \frac{W_5}{L_5}, \frac{W_6}{L_6}, \frac{W_7}{L_7}, I_T, \theta \right\}$$

$$\theta = \frac{I_{D6Q}}{I_{Tot}} = \frac{P_2}{P}$$

$$I_{Tot} = I_T + I_{D6Q}$$

$$A_O \cong \frac{g_{md}g_{mo}}{g_{oo}g_{od}} \quad \Rightarrow \quad A_O = \frac{2\sqrt{2}C_{OX}\sqrt{\mu_n\mu_p}\sqrt{\frac{W_1W_5}{L_1L_5}}}{(\lambda_n + \lambda_p)^2 I_T \sqrt{\frac{W_6L_7}{W_7L_6}}}$$

Consider the Natural Reduced Parameter Set

$$\left\{ \frac{W_1}{L_1}, \frac{W_3}{L_3}, \frac{W_5}{L_5}, \frac{W_6}{L_6}, \frac{W_7}{L_7}, I_T, \theta \right\}$$

$$GB \cong \frac{g_{md}}{C_C} \quad \Rightarrow \quad GB = \frac{\sqrt{\frac{\mu_n C_{OX} W_1}{L_1}} \sqrt{I_T}}{C_C}$$

$$SR \cong \frac{I_T}{C_C}$$

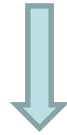
Constraint:

$$C_C = \frac{C_L \beta}{Q^2} \frac{g_{mo} g_{md}}{(g_{mo} - \beta g_{md})^2} \quad \Rightarrow \quad C_C = \frac{C_L \beta}{Q^2} \frac{\sqrt{\mu_n \mu_p} \sqrt{2 \frac{W_1 W_5 W_6 L_7}{L_1 L_5 L_6 W_7}}}{\left(\sqrt{2 \mu_p \frac{W_5 W_6 W_7}{L_5 L_6 L_7}} - \beta \sqrt{\mu_n \frac{W_1}{L_1}} \right)^2}$$

Consider the Natural Reduced Parameter Set

$$\left\{ \frac{W_1}{L_1}, \frac{W_3}{L_3}, \frac{W_5}{L_5}, \frac{W_6}{L_6}, \frac{W_7}{L_7}, I_T, \theta \right\}$$

$$V_{\text{inMIN}} = V_{T1} + V_{EB1} + V_{EB7} + V_{SS}$$



$$V_{\text{imin}} = V_{T1} + \sqrt{\frac{I_T L_1}{\mu_n C_{OX} W_1}} + \sqrt{\frac{2I_T L_7}{\mu_n C_{OX} W_7}} + V_{SS}$$

Expressions for remainder of signal swings are particularly complicated !

Observation

- Even the most elementary performance parameters require very complicated expressions when the natural design parameter space is used
- Strong simultaneous dependence on multiple natural design parameters
- Interdependence and notational complexity obscures insight into performance and optimization

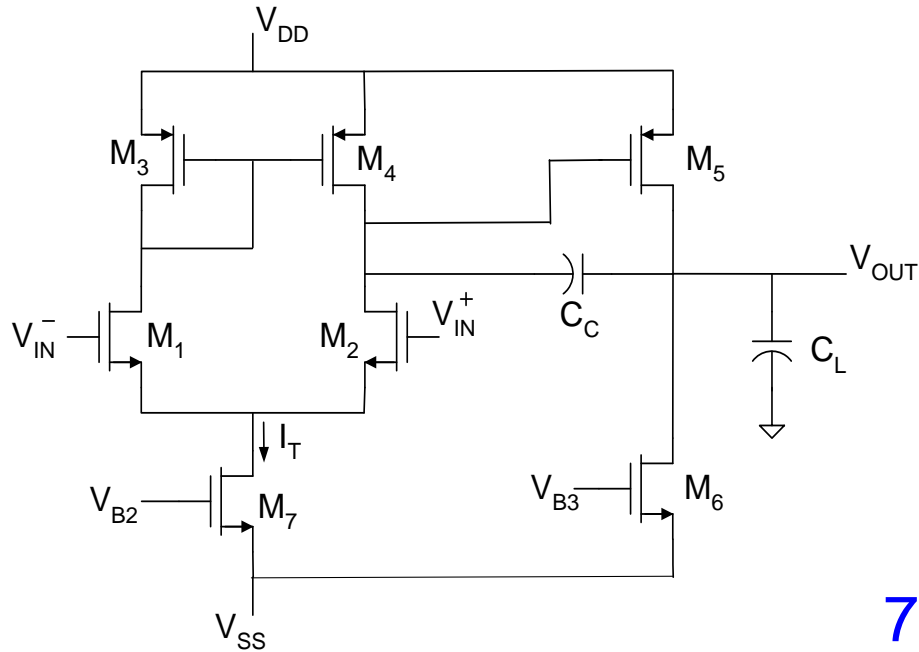
Practical Set of Design Parameters

$$S_{\text{PRACTICAL}} = \{P, \theta, V_{\text{EB}1}, V_{\text{EB}3}, V_{\text{EB}5}, V_{\text{EB}6}, V_{\text{EB}7}\}$$

7 degrees of freedom!

- P : total power dissipation
- θ = fraction of total power in second stage
- $V_{\text{EB}k}$ = excess bias voltage for the k^{th} transistor
- Phase margin constraint assumed (so C_C not shown in DoF)

Basic Two-Stage Op Amp



7 Degrees of Freedom


$\{P, \theta, V_{EB1}, V_{EB3}, V_{EB5}, V_{EB6}, V_{EB7}\}$



$\left\{ \frac{W_1}{L_1}, \frac{W_3}{L_3}, \frac{W_5}{L_5}, \frac{W_6}{L_6}, \frac{W_7}{L_7}, I_T, \theta \right\}$

Relationship Between the Practical Parameters and the Natural Design Parameters

$$\{P, \theta, V_{EB1}, V_{EB3}, V_{EB5}, V_{EB6}, V_{EB7}\}$$

$$\left\{ \frac{W_1}{L_1}, \frac{W_3}{L_3}, \frac{W_5}{L_5}, \frac{W_6}{L_6}, \frac{W_7}{L_7}, I_T, \theta \right\}$$


$$I_T = \frac{P(1-\theta)}{V_{DD}}$$

$$I_{DQi} \in \left\{ I_T, \frac{I_T}{2}, \frac{\theta P}{V_{DD}} \right\}$$

$$\left(\frac{W}{L} \right)_i \cong \frac{2I_{DQi}}{\mu_i C_{OX} V_{EBi}^2}$$

A Set of Independent Design Parameters is Needed

Consider Practical Parameter Set

$$\{P, \theta, V_{EB1}, V_{EB3}, V_{EB5}, V_{EB6}, V_{EB7}\}$$

$$A_o = \frac{4}{(\lambda_n + \lambda_p)^2 V_{EB1} |V_{EB5}|}$$

$$GB = \frac{P(1-\theta)}{V_{DD} V_{EB1} C_C} = \frac{PQ^2 (2\theta V_{EB1} - \beta(1-\theta) |V_{EB5}|)^2}{C_L \beta 2\theta V_{EB1}^2 |V_{EB5}| V_{DD}}$$

$$SR = \frac{PQ^2 (2\theta V_{EB1} - \beta(1-\theta) |V_{EB5}|)^2}{C_L \beta 2\theta V_{EB1} |V_{EB5}| V_{DD}}$$

Constraint:

$$C_C = \frac{C_L 2\theta(1-\theta)\beta}{Q^2} \frac{V_{EB1} |V_{EB5}|}{(V_{EB1} 2\theta - \beta |V_{EB5}| (1-\theta))^2}$$

Observation:

$$GB = \frac{P(1-\theta)}{V_{DD}V_{EB1}C_C} = \frac{PQ^2(2\theta V_{EB1} - \beta(1-\theta)|V_{EB5}|)^2}{C_L\beta 2\theta V_{EB1}^2|V_{EB5}|V_{DD}}$$

$$SR = \frac{PQ^2(2\theta V_{EB1} - \beta(1-\theta)|V_{EB5}|)^2}{C_L\beta 2\theta V_{EB1}|V_{EB5}|V_{DD}}$$

GB and SR are inter-related for this Op Amp

$$SR = V_{EB1} \cdot GB$$

Could have made this observation in the other parameter domains as well !

A Set of Independent Design Parameters is Needed

Consider Practical Parameter Set

$$\{P, \theta, V_{EB1}, V_{EB3}, V_{EB5}, V_{EB6}, V_{EB7}\}$$

$$V_{OMAX} = V_{DD} - |V_{EB5}|$$

$$V_{OMIN} = V_{SS} + V_{EB6}$$

$$V_{inMIN} = V_{T1} + V_{EB1} + V_{EB7} + V_{SS}$$

$$V_{inMAX} = V_{DD} - \max\{(|V_{EB3}| + |V_{T3}| - V_{T1}), (|V_{EB5}| + |V_{T5}| - V_{T2})\}$$

All expressions are quite manageable in the practical parameter domain except for the GB expression

Characteristics of the Practical Design Parameter Space

- Minimum set of independent parameters
- Results in major simplification of the key performance parameters
- Provides valuable insight which makes performance optimization more practical

Design Assumptions

- Assume the following system parameters:

$$V_{DD} = 3.3 \text{ V}$$

$$C_L = 1 \text{ pF}$$

- Typical 0.35um CMOS process
- Simulation corner: typ/55°C/3.3V

Example for Design Procedure

Given specifications:

$$A_0: 66\text{dB}$$

$$\text{GB}: 5\text{MHz}$$

$$V_{\text{OMIN}}=0.25\text{V}$$

$$V_{\text{OMAX}}=3.1\text{V}$$

$$V_{\text{INMIN}}=1.1\text{V}$$

$$V_{\text{INMAX}}=3\text{V}$$

$$P=0.17\text{mw}$$

$$\beta=1 \quad \text{with pole } Q=.707$$

Assume: $V_{\text{TN}} = 0.6$, $V_{\text{TP}} = -0.7$, $\lambda_n=0.04$, $\lambda_p=0.18$

7 constraints (in addition to φ_m) and 7 degrees of freedom

Example for Design Procedure

1. Choose channel length

2. $V_{EB3}, V_{EB5}, V_{EB6}$

$\{P, \theta, V_{EB1}, V_{EB3}, V_{EB5}, V_{EB6}, V_{EB7}\}$

$$V_{imax} = V_{DD} + V_{EB3} + V_{T1} + V_{T3}$$

$$V_{omax} = V_{DD} + V_{EB5}$$

$$V_{omin} = V_{EB6}$$

3. V_{EB1}

$$A_O = \frac{4}{(\lambda_n + \lambda_p)^2 V_{EB1} |V_{EB5}|}$$

$\{P, \theta, V_{EB1}, V_{EB3}, V_{EB5}, V_{EB6}, V_{EB7}\}$

4. V_{EB7}

$$V_{imin} = V_{EB1} + V_{EB7} + V_{T1}$$

$\{P, \theta, V_{EB1}, V_{EB3}, V_{EB5}, V_{EB6}, V_{EB7}\}$

5. Choose P to satisfy power constraint

$\{P, \theta, V_{EB1}, V_{EB3}, V_{EB5}, V_{EB6}, V_{EB7}\}$

(note this step could have occurred earlier since P is one of the design variables)

Example for Design Procedure

6. Choose θ to meet GB constraint

(the expression for GB really contains only one unknown at this stage, θ , though expression is not explicit since θ also appears in C_C)

~~$\{P, \theta, V_{EB1}, V_{EB3}, V_{EB5}, V_{EB6}, V_{EB7}\}$~~

$$GB = \frac{P(1-\theta)}{V_{DD}V_{EB1}C_C}$$

Must solve nonlinear equation in θ

7. Compensation capacitance C_C

$$C_C = \frac{C_L \beta}{Q^2} 2\theta(1-\theta) \frac{V_{EB1}|V_{EB5}|}{(V_{EB1}2\theta - \beta V_{EB5}(1-\theta))^2}$$

8. Calculate all transistor sizes

$$I_T = \frac{P(1-\theta)}{V_{DD}}$$

$$I_{5Q} = \frac{P\theta}{V_{DD}}$$

$$\frac{W_k}{L_k} = \frac{2I_{Dk}}{\mu_k C_{OX} V_{EBk}^2}$$

9. Implement structure, simulate, and make modifications if necessary guided by where deviations may occur

Note: It may be necessary or preferable to make some constraints an inequality

Note: Specifications may be over-constrained or have no solution

Note: Sequence of steps may change with different requirements for this amplifier

Example for Design Procedure

Summary of Design Procedure for This Set of Specifications and this Architecture:

1. Choose channel length
2. Select: V_{EB3} , V_{EB5} , V_{EB6}
3. Select: V_{EB1}
4. Select: V_{EB7}
5. Choose P to satisfy power constraint
6. Choose θ to meet GB constraint
7. Compensation capacitance C_C
8. Calculate all transistor sizes
9. Implement structure, simulate, and make modifications if necessary
guided by where deviations may occur

Note: Though not shown, this design procedure was based upon looking at the set of equations that must be solved and developing a sequence to solve these equations. It may not always be the case that equations can be solved sequentially.

Note: Different specification requirements (constraints) will generally require a different design procedure

Example for Design Procedure

Design results (with $L=2\mu\text{m}$):

$M_{1,2}$ W/L	$M_{3,4}$ W/L	M_5 W/L	M_6 W/L	M_7 W/L	P	θ	C_c
13/2	24.5/2	54/2	17.4/2	17.4/2	0.17mW	.51	3.7pF

Simulation results:

A0	GB	P	Phase margin
65dB	5.2MHz	.17mW	45.4 degrees

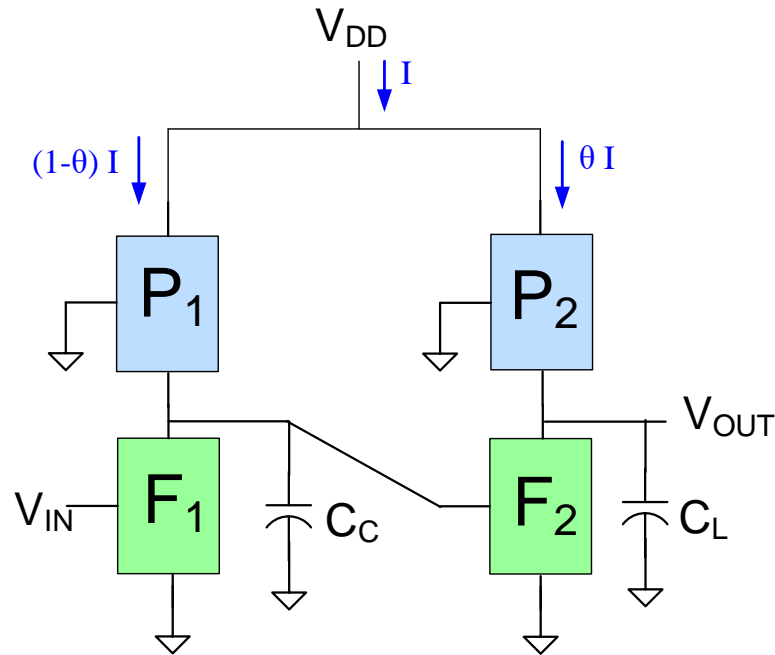
Spreadsheet for Design Space Exploration

Settling Characteristics of Two-Stage Operational Amplifier																						
Process Parameters																						
uCoxn		9E-05		In		0.02		Power	0.01													
uCoxp		5E-05		Ip		0.1		CT	1E-12													
Vtn		0.768						Vdd	4													
Vtp		0.774																				
Design Parameters					Performance Characteristics					Input Range				Output Range				Device Sizing				
VEB1	VEB2	VEB5	VEB6	VEB7	η	Ao	GB	ISS(mA)	CC	Vmin	Vmax	Vmir	Vmax	W/L1	W/L2	W/L5	W/L6	W/L7				
0.5	0.5	0.5	0.25	0.25	0.5	1111	8.3E+08	1.67	4E-12	1.52	4.27	0.25	3.5	72.5	148.1	148.1	289.9	579.7				
1	0.5	0.5	0.25	0.25	0.5	556	1.9E+09	1.67	8.9E-13	2.02	4.27	0.25	3.5	18.1	148.1	148.1	289.9	579.7				
2	1	0.5	0.25	0.25	0.5	278	2.6E+09	1.67	3.3E-13	3.02	3.77	0.25	3.5	4.5	37.0	148.1	289.9	579.7				
0.5	1	0.5	0.25	0.25	0.5	1111	8.3E+08	1.67	4E-12	1.52	3.77	0.25	3.5	72.5	37.0	148.1	289.9	579.7				
1	2	0.5	0.25	0.25	0.5	556	1.9E+09	1.67	8.9E-13	2.02	2.77	0.25	3.5	18.1	9.3	148.1	289.9	579.7				
2	2	0.5	0.25	0.25	0.5	278	2.6E+09	1.67	3.3E-13	3.02	2.77	0.25	3.5	4.5	9.3	148.1	289.9	579.7				
0.5	0.5	1	0.25	0.25	0.5	556	ERR	1.67	ERR	1.52	4.27	0.25	3	72.5	148.1	37.0	289.9	579.7				
1	0.5	1	0.25	0.25	0.5	278	4.2E+08	1.67	4E-12	2.02	4.27	0.25	3	18.1	148.1	37.0	289.9	579.7				
2	1	1	0.25	0.25	0.5	139	9.4E+08	1.67	8.9E-13	3.02	3.77	0.25	3	4.5	37.0	37.0	289.9	579.7				
0.5	1	1	0.25	0.25	0.5	556	ERR	1.67	ERR	1.52	3.77	0.25	3	72.5	37.0	37.0	289.9	579.7				
1	2	1	0.25	0.25	0.5	278	4.2E+08	1.67	4E-12	2.02	2.77	0.25	3	18.1	9.3	37.0	289.9	579.7				
2	2	1	0.25	0.25	0.5	139	9.4E+08	1.67	8.9E-13	3.02	2.77	0.25	3	4.5	9.3	37.0	289.9	579.7				
0.5	0.5	2	0.25	0.25	0.5	278	8.3E+08	1.67	4E-12	1.52	4.27	0.25	2	72.5	148.1	9.3	289.9	579.7				
1	0.5	2	0.25	0.25	0.5	139	ERR	1.67	ERR	2.02	4.27	0.25	2	18.1	148.1	9.3	289.9	579.7				

Summary

1. Determination of Design Space and Degrees of Freedom Often Useful for Understanding the Design Problem
2. Analytical Expressions for Key Performance Parameters give Considerable Insight Into Design Potential
3. Natural Design Parameters Often Not Most Useful for Providing Insight or Facilitating Optimization
4. Concepts Readily Extend to other Widely Used Structures

Power distribution between stages

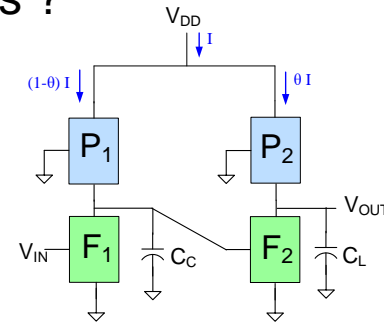


How should the power be split between the two stages ?

- Would often like to minimize power for a given speed (GB) requirement
- Optimal split may depend upon architecture

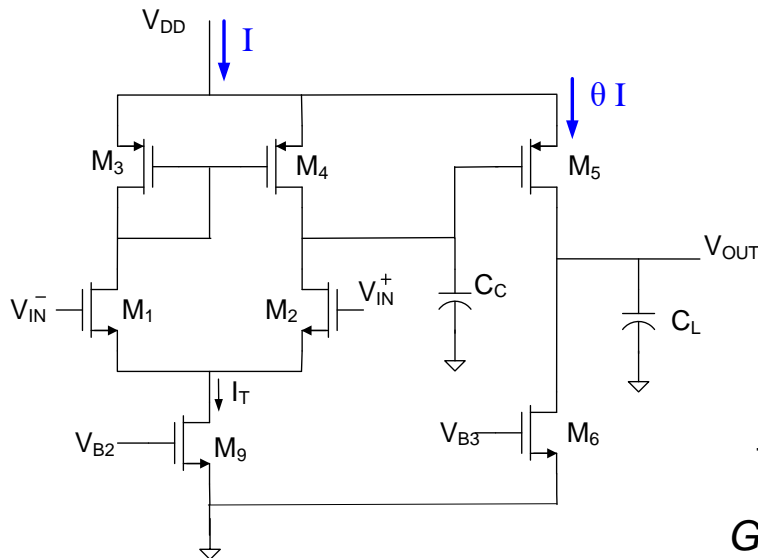
Power distribution between stages

How should the power be split between the two stages ?



Consider basic two-stage with first-stage compensation

Assume compensated with $p_2 = 3\beta A_0 p_1$



$$A_{10} = \frac{-g_{m1}}{g_{01} + g_{03}}$$

$$A_{20} = \frac{-g_{m5}}{g_{05} + g_{06}}$$

$$p_1 = \frac{g_{01} + g_{03}}{C_C}$$

$$p_2 = \frac{g_{05} + g_{06}}{C_L}$$

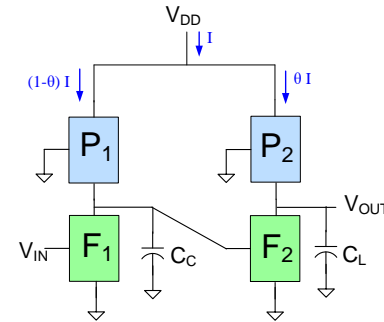
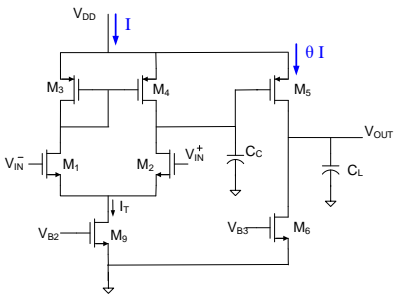
$$GB = A_{01} A_{02} p_1$$

thus

$$GB = \frac{g_{m1}}{g_{01} + g_{03}} \frac{g_{m5}}{g_{05} + g_{06}} \frac{g_{01} + g_{03}}{C_C} = \frac{g_{m1} g_{m5}}{(g_{05} + g_{06}) C_C}$$

Power distribution between stages

How should the power be split between the two stages to minimize power for given GB ?



Since $p_2 = 3\beta A_0 p_1$

Since $GB = \frac{g_{m1}g_{m5}}{(g_{05} + g_{06})C_C}$

$$\left. \begin{aligned} A_{10} &= \frac{-g_{m1}}{g_{01} + g_{03}} \\ A_{20} &= \frac{-g_{m5}}{g_{05} + g_{06}} \\ p_1 &= \frac{g_{01} + g_{03}}{C_C} \\ p_2 &= \frac{g_{05} + g_{06}}{C_L} \end{aligned} \right\}$$

$$\frac{g_{05} + g_{06}}{C_L} = 3\beta \frac{g_{m1}}{g_{01} + g_{03}} \frac{g_{m5}}{g_{05} + g_{06}} \frac{g_{01} + g_{03}}{C_C}$$

$$\frac{g_{05} + g_{06}}{C_L} = 3\beta \frac{g_{m1}g_{m5}}{C_C(g_{05} + g_{06})}$$

$$GB = \frac{g_{05} + g_{06}}{3\beta C_L}$$

$$GB = \frac{(\lambda_p + \lambda_n)\theta I}{3\beta C_L}$$

Finally $GB = \frac{(\lambda_p + \lambda_n)\theta P}{V_{DD} 3\beta C_L}$

Thus for given GB, for this structure want θ as close to 1 as is practical

Power distribution between stages

Note: Optimum power split for previous example was for dominant pole compensation in first stage. Results may be different for Miller compensation or for output compensation

For first-stage compensation capacitor with compensation criteria $p_2 = 3\beta A_0 p_1$:

$$GB = \frac{(\lambda_p + \lambda_n)\theta P}{V_{DD} 3\beta C_L}$$

For Miller Compensation with RHP zero and arbitrary Q compensation criteria:

$$GB = \frac{P(1-\theta)}{V_{DD} V_{EB1} C_C} = \frac{PQ^2 (2\theta V_{EB1} - \beta(1-\theta) |V_{EB5}|)^2}{C_L \beta 2\theta V_{EB1}^2 |V_{EB5}| V_{DD}}$$

By taking derivative of GB wrt θ , it can be easily shown that the derivative is positive in the interval $0 < \theta \leq 1$ indicating that for a given P, want to make θ close to 1 to maximize GB



Stay Safe and Stay Healthy !

End of Lecture 17